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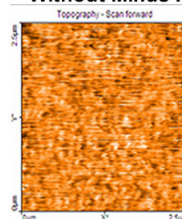
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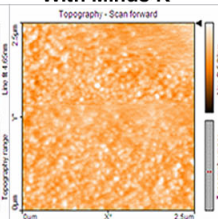
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Metal-oxide complementary inverters with a vertical geometry fabricated on flexible substrates

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We report on the fabrication of *p*-channel thin film transistors (TFTs) and vertically stacked complementary inverters comprised of a *p*-channel copper oxide TFT on top of an *n*-channel indium gallium zinc oxide TFT fabricated on a flexible polyethersulfone substrate. The *p*- and *n*-channel TFTs showed saturation mobility values of 0.0022 and 1.58 cm²/Vs, respectively, yielding inverters with a gain of 120 V/V. This level of performance was achieved by reducing the copper oxide channel thickness, allowing oxygen diffusion into the copper oxide layer at medium processing temperature (150 °C). © 2011 American Institute of Physics. [doi:10.1063/1.3656974]

The realization of large-area electronic circuits on flexible substrates will require thin-film transistor (TFT) technologies fabricated at much lower temperatures than amorphous silicon or poly-silicon TFTs. Metal-oxide semiconductor TFTs are one candidate to implement such flexible electronics because they can be processed at low-temperature and potentially could be air-stable and have high carrier mobility.¹ However semiconducting metal-oxides are commonly electron conductors as their intrinsic anion-deficiency creates an overlap of metal *s* orbitals at the bottom of the conduction band that facilitates carrier transport and results in high electron mobility.^{1,2}

A smaller number of metal-oxides are cation-deficient and potentially hole conductors. In most of them, the upper valence band is populated by oxygen 2*p* states that create a strong Coulomb force, resulting in the deep level localization of holes.^{3–5} In copper oxide however, Cu 3*d* states dominate the upper valence band, and by hybridization with oxygen *s* states,^{4,6} they create less localized holes. The holes are also created as Cu(I) is oxidized to Cu(II) through excess oxygen.^{2,4,6,7} The hole mobility value, however, is much lower than electron mobility in metal-oxides. A major challenge in realizing high performance *p*-channel TFTs is then to find the processing conditions which allow the oxide layer to act as a *p*-channel semiconductor rather than a conductor or an insulator. Annealing has been recognized as a critical step because it promotes oxygen diffusion into the metal oxide layer where it can suppress oxygen vacancies and promote the oxidation of metal atoms. Both processes reduce the carrier density allowing the channel to be less conductive and the transistor to achieve low off currents at zero gate voltages or at low drain to source voltages. *P*-channel TFTs have been demonstrated with copper oxide, but the fabrication processes were generally performed at temperatures that are too high for plastic substrates (200 °C).^{8–11} copper oxide TFTs annealed at 200 °C showed saturation mobility values in the range of 10^{−3} cm²/Vs.^{8,11} Higher mobilities values of

4.8 cm²/Vs have also been reported in *p*-channel tin oxide TFTs also annealed at 200 °C.¹⁰

Although metal-oxide inverters have been reported previously,^{12–14} only a few are complementary. These complementary inverters were fabricated on silicon substrates because of their high processing temperature (200 °C) and their performance was limited with maximum gain values around 11 V/V.^{12,13} In general, this level of performance can be attributed to the poor transistor characteristics of the *p*-channel TFT and to unbalanced electron and hole mobilities. However, we have recently demonstrated a vertically stacked inverter geometry that allows for independent control over the thicknesses of the gate dielectrics and over the channel/dielectric critical interfaces of each TFT.^{15,16}

Here, we demonstrate the fabrication of *p*-channel metal-oxide TFTs at low-temperature (<150 °C) and high-gain metal-oxide vertically stacked complementary inverters on flexible polyethersulfone (PES) substrates. The inverters are comprised of a top-contact *p*-channel copper oxide TFTs fabricated on top of a bottom-contact *n*-channel amorphous-InGaZnO (α -IGZO) TFT with a common gate electrode. The *p*- and *n*-channel TFTs yielded saturation field-effect mobility values of 0.0022(±0.0003) and 1.58(±0.18) cm²/Vs and threshold voltage values of −4.75(±1.04) and 5.77(±0.61) V, respectively. The average values were measured in four identical devices of each type. The best complementary inverter yielded a static dc gain value of 120 V/V with a switching threshold voltage of 7.5 V at a supply voltage of 20 V.

The devices were fabricated on 3.8 × 3.8 cm² PES substrates. First, bottom source and drain electrodes, a 6 nm-thick titanium (Ti) layer followed by a 80 nm-thick gold (Au) layer, were deposited through shadow mask using electron-beam deposition system (Denton Explorer). Then, a 30 nm-thick α -IGZO channel layer (Ga₂O₃:In₂O₃:ZnO = 1:1:1 mol. %) was deposited through shadow mask without intentionally heating of the substrate using PVD-75 radio-frequency (rf)-sputterer at 125 W power and 5 mTorr (0.67 Pa) deposition pressure with argon (Ar) and oxygen (O₂) pressure ratios of 98% and 2%, respectively. The length and width of the *n*-channel active layer were 180 μm and 400 μm, respectively.

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Then, a 150 nm-thick Al_2O_3 was grown using atomic layer deposition (ALD) at 110°C . Next, the common gate electrode, a 6 nm-thick nickel (Ni) followed by a 90 nm-thick Au and another 6 nm-thick Ni layer, was deposited through shadow mask using an e-beam evaporator. Next, another 75 nm-thick Al_2O_3 layer was deposited using ALD at 110°C . Then, a 10 nm-thick copper oxide channel layer (99.995% purity) was deposited through shadow mask without intentionally heating the substrate using rf-sputterer at a power of 50 W and 10 mTorr (1.33 Pa) deposition pressure with Ar and O_2 pressure ratios of 95% and 5%, respectively. The length and width of the p -channel active layer were $180\ \mu\text{m}$ and $4000\ \mu\text{m}$, respectively. Finally, the top source and drain electrodes, a 6 nm-thick Ni layer followed by a 90 nm-thick Au layer, were deposited through shadow mask using an e-beam evaporator. After fabrication, the output and transfer characteristics of the individual TFTs and the voltage transfer curves of the inverters were measured using an Agilent E5272 medium-power source/monitor unit connected to a probe station. The capacitance density values for the 150 and 75 nm-thick Al_2O_3 layers were measured to be 54 and $108\ \text{nF}/\text{cm}^2$, respectively.

The diffusion of oxygen into the oxide layer during annealing is a thermally promoted process but is also affected by the porosity and the path-length for the gas to diffuse into the solid film. At low annealing temperatures, the kinetics of this process is expected to be slower and limited by the morphology of the films (including film thickness, porous size, etc.). To facilitate the diffusion process at lower temperatures, the thickness of the copper oxide layer must be reduced to allow oxygen to diffuse down and reach to the channel-dielectric interface. Figures 1(a) and 1(b) show the output and transfer characteristics, respectively, of copper oxide TFTs with different layer thickness annealed for 30 min at 150°C using an ADP-120 oven, filled with O_2 at 150 Torr (0.02 MPa). The O_2 saturated ambient is used to facilitate the diffusion process compared to annealing in air. As it is clear from these

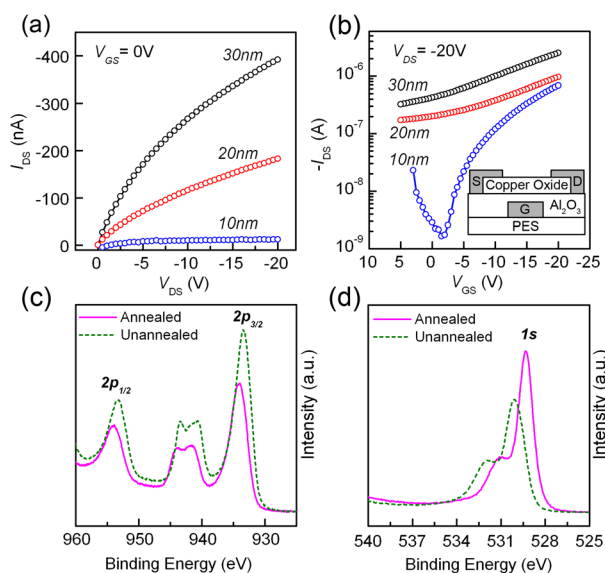


FIG. 1. (Color online) Representative (a) output characteristics ($I_{DS} - V_{DS}$) at zero gate voltage (V_{GS}), representative (b) I_{DS} vs. V_{GS} at $V_{DS} = -20\text{V}$ of three TFTs with different channel thicknesses of 10, 20, and 30 nm, (c) Cu 2p, and (d) O 1s XPS peaks of not-annealed and oxygen annealed copper oxide devices.

figures, devices with thickness above 10 nm exhibit conductive channels that can be modulated but not turned off completely with the gate voltage. TFTs with thicker channel layers show off-current values around two orders of magnitude higher than optimized devices. Figures 1(c) and 1(d) show the Cu 2p and O 1s X-ray photoelectron spectroscopy (XPS) spectra before and after annealing of an 8 nm-thick copper oxide film. Both XPS spectra are similar, with peaks at binding energies corresponding to CuO and Cu_2O peaks reported in the literature,^{11,17} indicating the coexistence of both phases. Upon annealing, the binding energies of the Cu 2p and O 1s peaks undergo shifts which are consistent with the oxidation of Cu^+ to Cu^{2+} .¹⁷ While this result suggests an increased CuO concentration, from this data, it is unclear if Cu_2O phases remain in the film. Furthermore, X-ray diffraction experiments in these films did not yield any distinguishable peaks likely due to its small thickness and the sensitivity of our equipment. While further studies are still needed to clarify the composition and structure of these films, it is clear from the current-voltage characteristics of the copper oxide TFTs shown in Figs. 1(a) and 1(b) that the combination of thinner films and the low temperature annealing here proposed is effective in reducing the conductivity of copper oxide to the point where it can be used as an effective p-type semiconductor.

The geometry of the inverter is shown in Fig. 2(a). Representative hysteresis transfer and single sweep output characteristic are shown in Figs. 2(b) and 2(c) for the p-channel TFTs and in Figs. 2(d) and 2(e) for the n-channel TFTs in the inverter structure. Saturation mobility values of 0.0022 and $1.58\ \text{cm}^2/\text{Vs}$ and threshold voltage values of -4.75 and

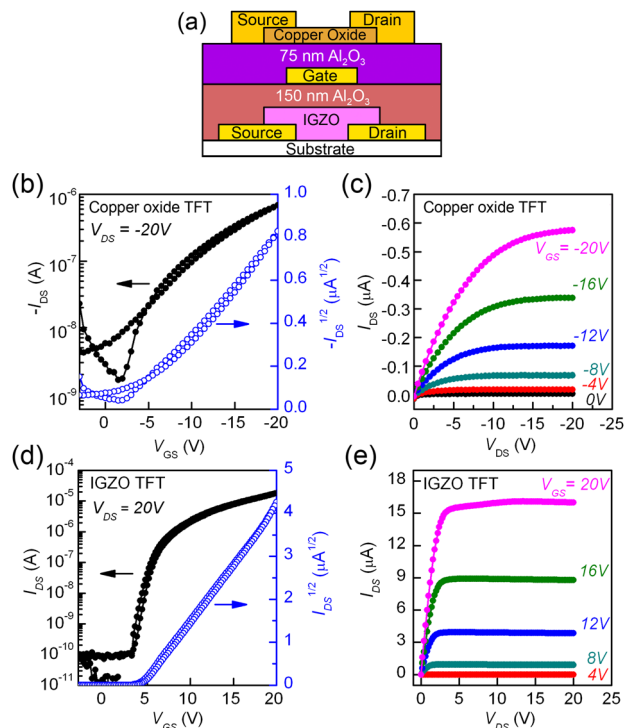


FIG. 2. (Color online) (a) Schematic of a vertically stacked p -channel copper oxide transistor fabricated on top of an n -channel α -IGZO transistor on a flexible PES substrate. Representative (b) hysteresis transfer and (c) single sweep output characteristics of copper oxide p -channel TFTs with $W_p = 4000\ \mu\text{m}$ and $L_p = 180\ \mu\text{m}$. Representative (d) hysteresis transfer and (e) single sweep output characteristics of α -IGZO n -channel TFTs with $W_n = 400\ \mu\text{m}$ and $L_n = 180\ \mu\text{m}$.

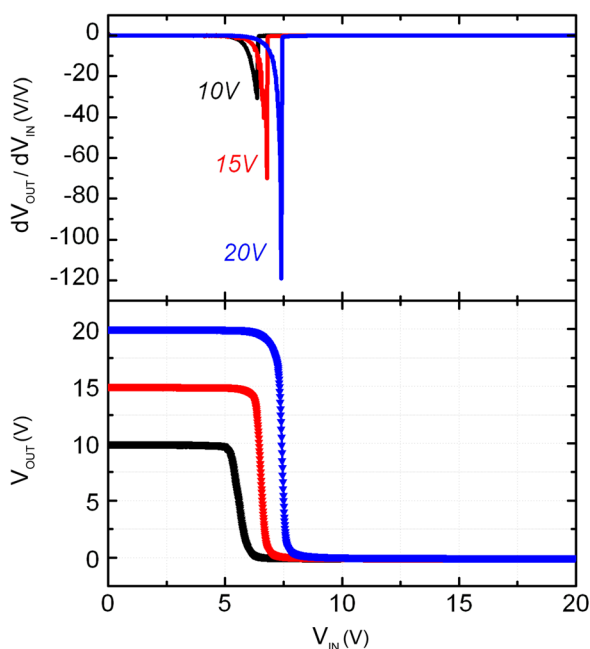


FIG. 3. (Color online) Voltage transfer characteristics and static DC gains of the inverter at different supply voltages of 5, 10, and 20 V.

5.77 V were estimated for the p - and n -channel TFTs, respectively. We note that the p -channel mobility value is of the same order of magnitude as previously reported in the literature for copper oxide TFTs processed at higher temperatures.⁹ Furthermore, the current on-off ratio of these p -channel TFTs, 3.9×10^2 , is slightly larger than previously reported literature values.⁸ Further reductions of the off-current on both types of transistors can also be expected by patterning their channel layers.

The shadow masks at our disposal limited our choices of channel aspect ratios, making the on-currents between both types of transistors unbalanced. However, the good performance of both transistors still allowed for a proof-of-principle demonstration of complementary inverters by connecting the vertically stacked n - and p -channel TFTs as shown in the inset of Fig. 2(a). The static performance of an inverter is evaluated by its static circuit gain and noise margin values extracted from the measured inverter voltage transfer characteristics (VTCs).^{15,16} Figure 3 shows the VTCs and static DC gain values (dV_{OUT}/dV_{IN}) of the inverters at different supply voltages (V_D) of 5, 10, and 20 V, respectively. At 20 V, the complementary inverter yielded a high gain value of -120 V/V and a V_M of 7.48 V with noise margin low and noise margin high values of 6.01 and 11.68 V, respectively, with a steepness value of $\Delta V_{IN} = 1.29$ V (6.45% of maximum V_{IN}). The performance of the inverter is summarized in Table I. Although the inverter reached considerably high gain values, unbalanced noise margins were obtained due to the large difference between the on-currents of the p - and n -channel TFTs. To address this issue, the aspect ratio between the n -channel and p -channel widths as well as the dielectric thicknesses will have to be further adjusted, to compensate the difference in mobility values and optimize the inverter performance.

In summary, we have demonstrated the low-temperature processing of p -channel TFTs and vertically stacked comple-

TABLE I. Performance of a vertically stacked complementary inverter with a p -channel copper oxide TFT ($W_p = 4000 \mu\text{m}$, $L_p = 180 \mu\text{m}$) fabricated on top of an n -channel α -IGZO TFT ($W_n = 400 \mu\text{m}$, $L_p = 180 \mu\text{m}$) with different supply voltage ranges.

V_{IN} (V)	V_D (V)	A_V (V)	V_M (V)	NM_L (V)	NM_H (V)	ΔV_{IN} (V)
0 to +5	+5	-30	6.1	5.28	3.39	1.07
0 to +10	+10	-70	6.6	5.57	7.61	1.12
0 to +20	+20	-120	7.5	6.01	11.68	1.29

mentary inverters on flexible PES substrates. Reducing the channel thickness along with oxygen annealing at low temperature allowed the fabrication of p -channel copper-oxide TFTs with considerably better performance compare to previously reported devices obtained at high temperature. The p - and n -channel TFTs showed significant differences in saturation mobility values but low off-currents and high on-off ratios. A vertically stacked complementary inverter using such TFTs yielded a high gain value. While the vertically stacked geometry should allow for further optimization of the performance of such inverters, this work demonstrates that it will be possible to implement complementary circuits based on metal-oxide semiconductors on flexible substrates.

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